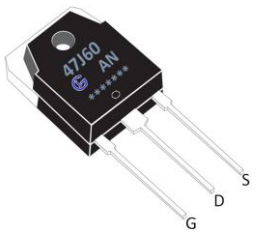
GL Silicon N-Channel Super-Junction Power MOSFET

$V_{DSS}(T_C=150℃)$	600	V
I_D	47	A
$P_D(T_C=25℃)$	400	W
$R_{DS(ON)}$	80	mΩ

General Description :

GL47J60AN the silicon N-channel Enhanced VDMOSFETS, is obtained by the self-aligned Superjunction Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-3P(N), which accords with the RoHS standard.

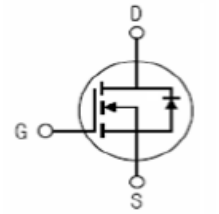
TO-3P(N)



Features :

- Proprietary New Super-Junction Technology
- $R_{DS(ON).typ.}$=0.08Ω
- Low Gate Charge Minimize Switching Loss
- 100% Single Pulse avalanche energy Test

Inner Equivalent Principium Chart



Applications :

- Adaptor
- Charger
- SMPS Standby Power
- Switching Voltage Regulators

Absolute (T_c=25℃unless otherwise specified) :

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	600	V
I_D	Continuous Drain Current	47	A
I_{DM}	Pulsed Drain Current	140	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy	1100	mJ
P_D	Power Dissipation	400	W
	Derating Factor above 25°C	3.23	W/℃
T_J , T_{stg}	Operating Junction and Storage Temperature Range	150 , −55 to 150	℃
T_L	MaximumTemperature for Soldering	300	℃

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

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Electrical Characteristics (Tc= 25℃ unless otherwise specified) :

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V,I_D=250μA	600	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=600V, V_{GS}=0V,T_a=25℃	--	--	1	μA
		V_{DS}=480V, V_{GS}=0V,T_a=125℃	--	--	100	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=+30V	--	--	10	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=-30V	--	--	-10	μA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=20A	--	80	95	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2.0	--	4.0	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=47A	--	40	--	S
Pulse width tp≤380μs,δ≤2%						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	V_{GS}= 0V V_{DS}=50V f=1.0MHz	--	4300	--	pF
C_{oss}	Output Capacitance		--	30	--	
C_{rss}	Reverse Transfer Capacitance		--	400	--	
Q_g	Total Gate Charge	I_D=47A,V_{DD}=480V V_{GS}=0 to 10V	--	115	--	nc
Q_{gs}	Gate to Source Charge		--	19	--	nc
Q_{gd}	Gate to Drain (“Miller”)Charge		--	40	--	nc

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	V_{DD}=300V,I_D=47A, V_{GS}=10V R_g=25Ω	--	96	--	nS
t_r	Rise Time		--	216	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	352	--	
t_f	Fall Time		--	100	--	

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Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	47	A
I_{SM}	Maximum Pulsed Current(Body Diode)		--	--	140	A
V_{SD}	Diode Forward Voltage	I_S=47A,V_{GS}=0V	--	--	1.5	V
t_{rr}	Reverse Recovery Time	V_R=480V, I_F=I_S, diF/dt=100A/us,V_{GS}=0V	--	520	--	ns
Q_{rr}	Reverse Recovery Charge		--	13	--	uC
Pulse width tp≤380μs,δ≤2%						

Symbol	Parameter	Max.	Units
$R_{\theta JC}$	Junction-to-Case	0.31	℃/W
$R_{\theta JA}$	Junction-to-Ambient	55	℃/W

TJ=+25℃ to +150℃

Pulse width≤380μs; duty cycle≤2%.

Characteristics Curve

Figure 1. Output Characteristics

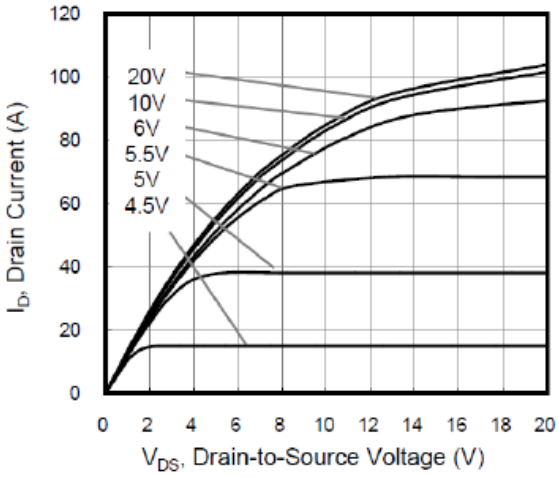


Figure 2. Transfer Characteristics

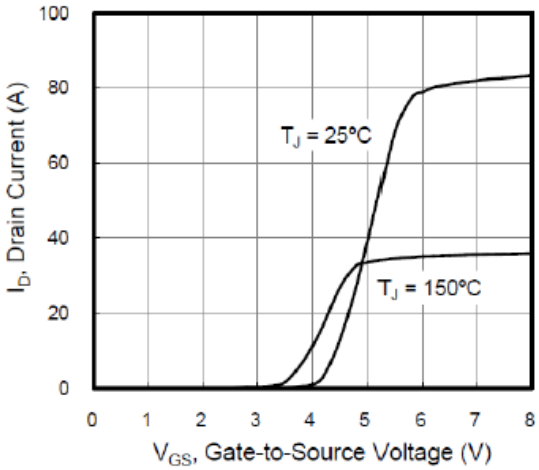


Figure 3. On-Resistance vs. Drain Current

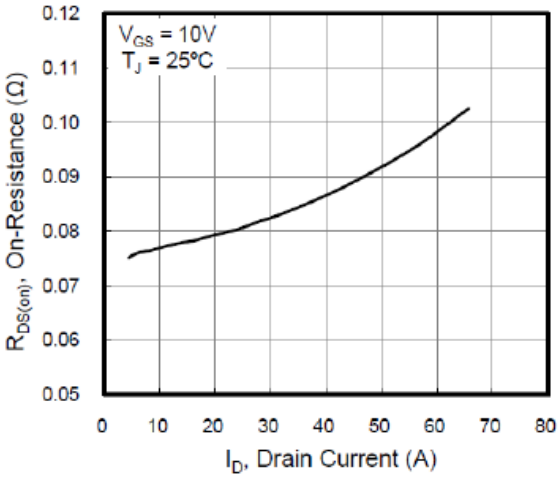


Figure 4. Capacitance

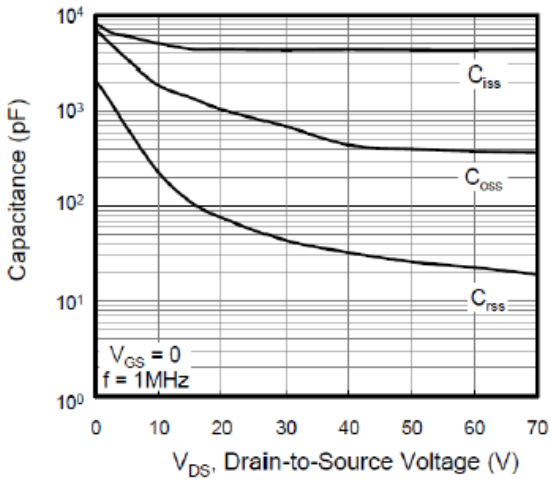


Figure 5. Gate Charge

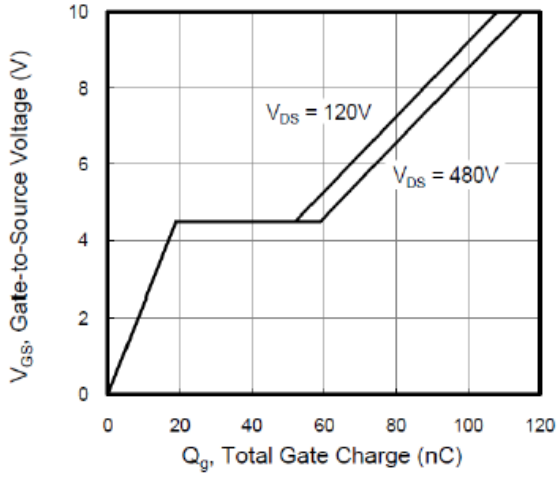


Figure 6. Body Diode Forward Voltage

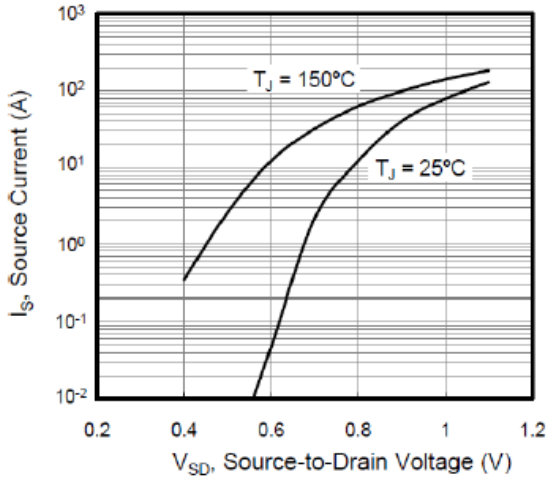


Figure 7. On-Resistance vs. Temperature

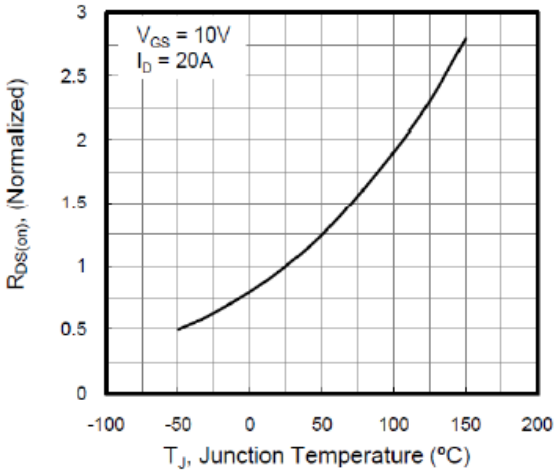


Figure 8. Threshold Voltage vs. Temperature

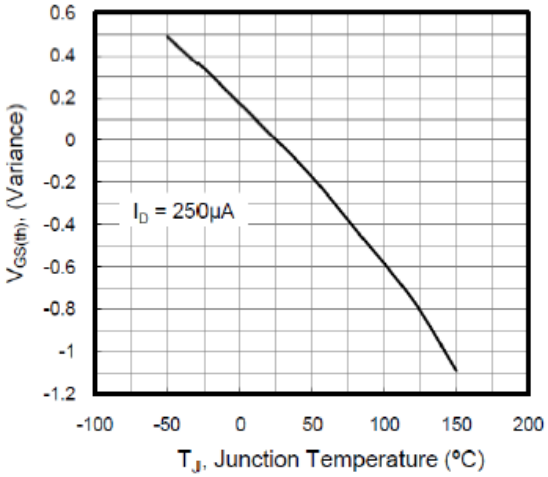


Figure 9. Transient Thermal Impedance

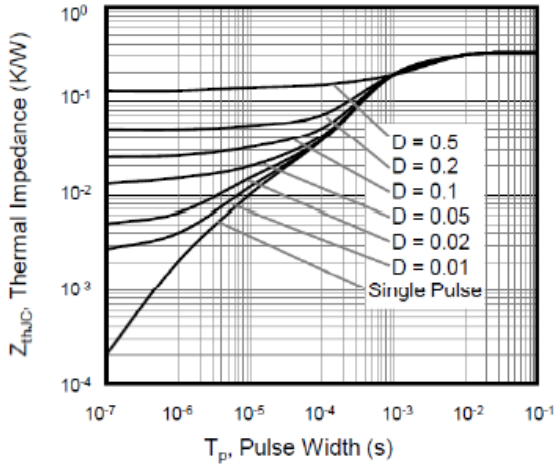
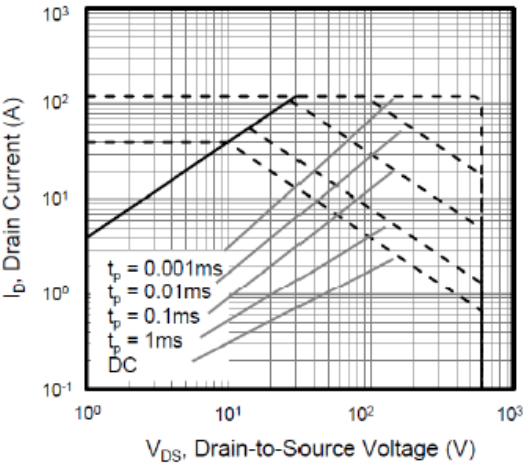


Figure 10. Safe Operating Area



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