

GL Silicon N-Channel Super-Junction Power MOSFET

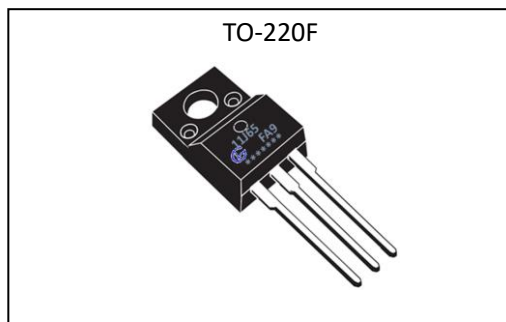
General Description :

GL11J65FA9, the silicon N-channel Enhanced MOSFETs, is obtained by the super junction technology which reduces the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package type is TO-220F, which accords with the RoHS standard.

V_{DS}	650	V
I_D	11	A
$P_D(T_C=25^{\circ}C)$	33	W
$R_{DS(ON)}$	0.35	Ω

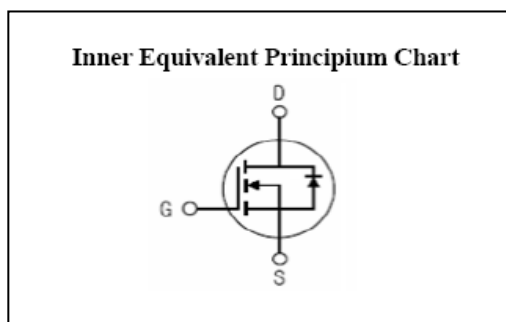
Features :

- Fast Switching
- Low Gate Charge
- Low Reverse transfer capacitances
- 100% Single Pulse avalanche energy Test



Applications :

- Power switch circuit of adaptor and charger.



Absolute ($T_C = 25^{\circ}C$ unless otherwise specified) :

Symbol	Parameter	Rating	Units
V_{DS}	Drain-to-Source Voltage	650	V
I_D	Continuous Drain Current	11	A
I_{DM}^{a1}	Pulsed Drain Current	33	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}^{a2}	Single Pulse Avalanche Energy	300	mJ
P_D	Power Dissipation	33	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	$-55+150$	$^{\circ}C$

**GL Silicon N-Channel Super-Junction Power MOSFET****Electrical Characteristics** ($T_c = 25^\circ\text{C}$ unless otherwise specified) :**OFF Characteristics**

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	650	--	--	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=650V, V_{GS}=0V, T_a=25^\circ\text{C}$	--	--	1	μA
		$V_{DS}=520V, V_{GS}=0V, T_a=125^\circ\text{C}$	--	--	100	
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+30V$	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-30V$	--	--	-100	nA

ON Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10V, I_D=6A$	--	0.3	0.35	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0		4	V

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=6A$	--	7.5	--	S
C_{iss}	Input Capacitance	$V_{GS}=0V, V_{DS}=50V$ $f=1.0\text{MHz}$	--	1050	--	pF
C_{oss}	Output Capacitance		--	90	--	
C_{rss}	Reverse Transfer Capacitance		--	4.8	--	

Resistive Switching Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D=6A, V_{DD}=520V$ $R_G=25\Omega$	--	12		ns
t_r	Rise Time		--	5		
$t_{d(OFF)}$	Turn-Off Delay Time		--	45		
t_f	Fall Time		--	5		
Q_g	Total Gate Charge	$I_D=6A, V_{DD}=520V$ $V_{GS}=10V$	--	25	--	nC
Q_{gs}	Gate to Source Charge		--	6.2	--	
Q_{gd}	Gate to Drain ("Miller") Charge		--	10	--	

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Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--		11	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--		33	A
V_{SD}	Diode Forward Voltage	$I_S=11A, V_{GS}=0V$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_F=I_S, I_F/dt=100A/us$	--	260		ns
Q_{rr}	Reverse Recovery Charge		--	3.1		uC

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case	2.71	°C/W
$R_{\theta JA}$	Junction-to-Ambient	75	°C/W

^{a1} : Repetitive rating; pulse width limited by maximum junction temperature

^{a2} : $L=10.0mH$, $R_g=25\ \Omega$, $V_{dd}=50V$, Start $T_j=25^\circ C$

Test Circuit and Waveform

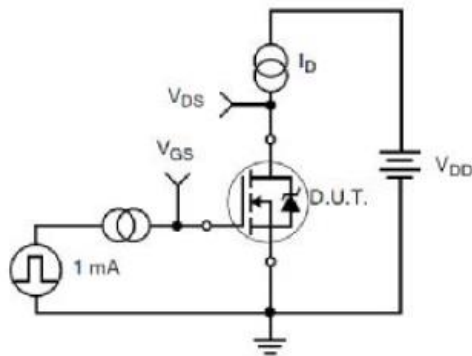


Figure 17. Gate Charge Test Circuit

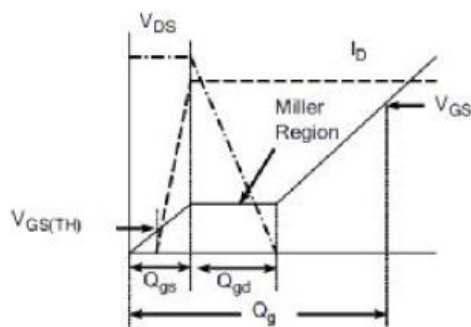


Figure 18. Gate Charge Waveform

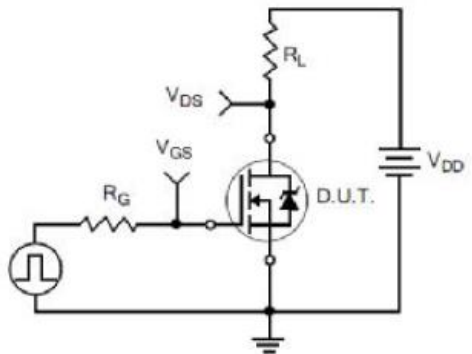


Figure 19. Resistive Switching Test Circuit

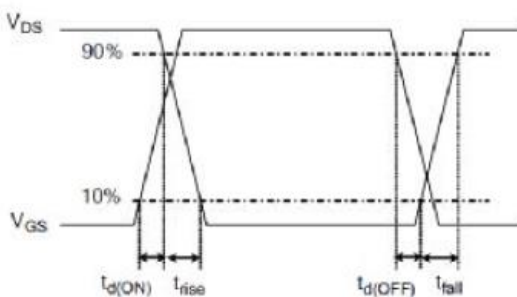


Figure 20. Resistive Switching Waveforms

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Typical Characteristics

Figure1. Safe operating area

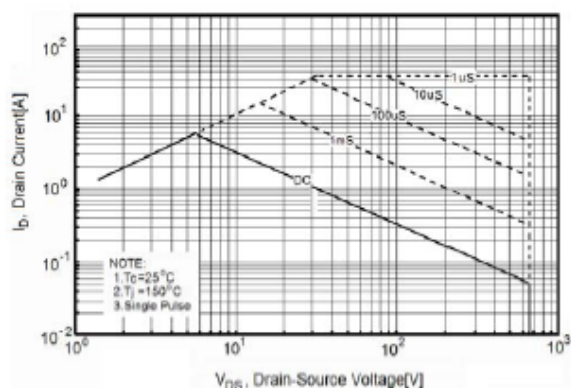


Figure2. Transient Thermal Impedance

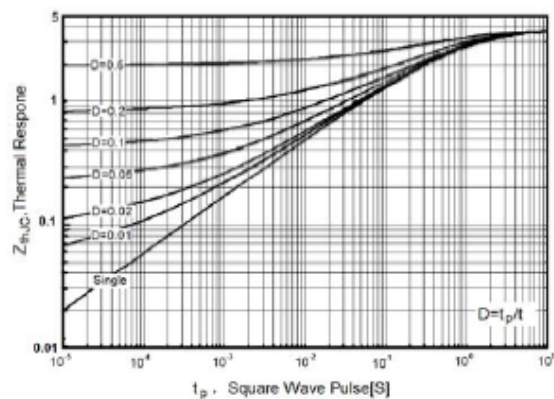


Figure3. Source-Drain Diode Forward Voltage

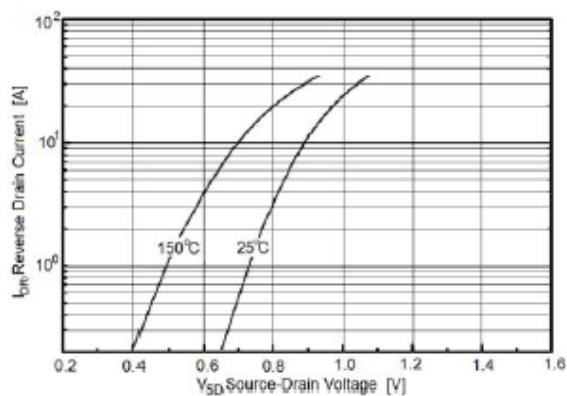


Figure4. Output characteristics

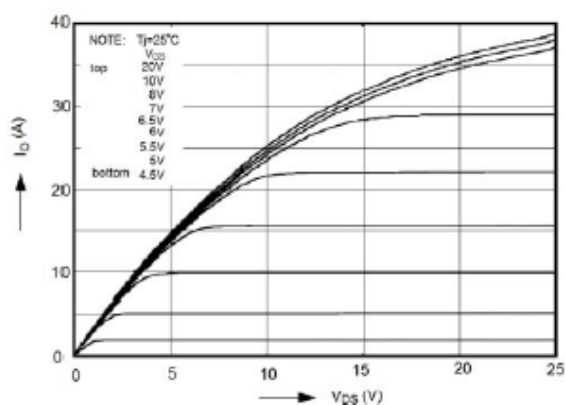


Figure5. Transfer characteristics

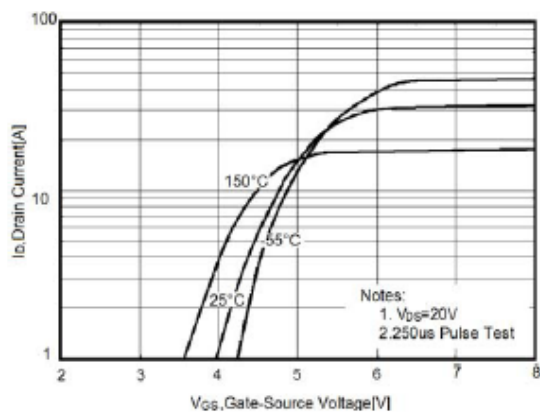
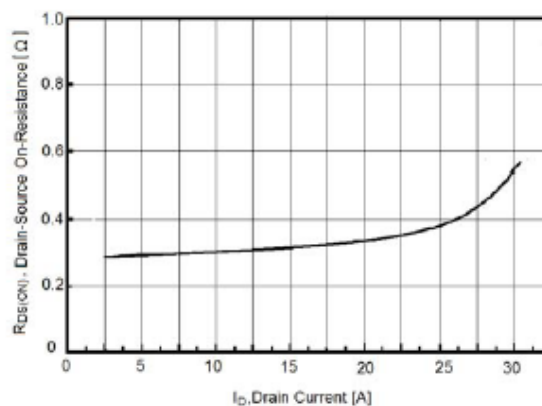


Figure6. Static drain-source on resistance



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Figure7. $R_{DS(ON)}$ vs Junction Temperature

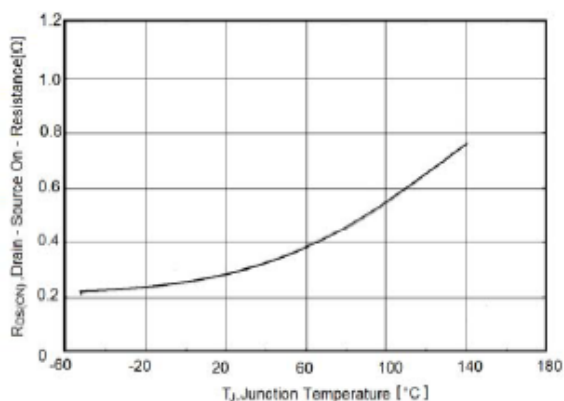


Figure8. BV_{DSS} vs Junction Temperature

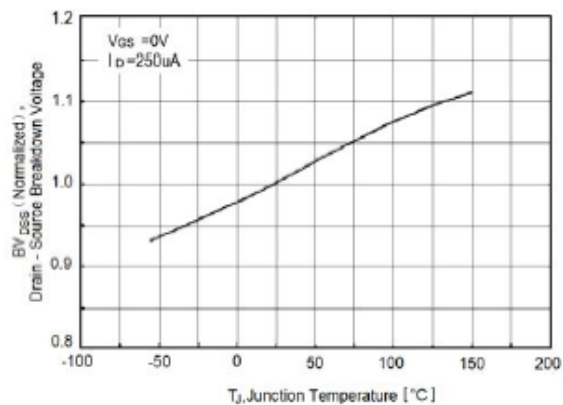


Figure9. Maximum I_D vs Junction Temperature

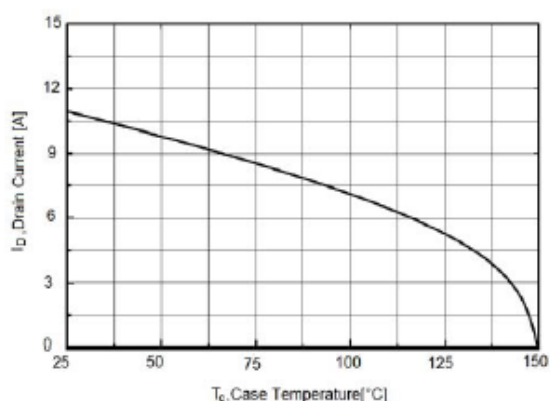


Figure10. Gate charge waveforms

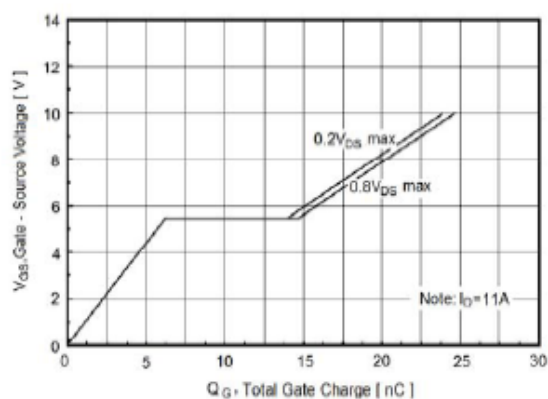


Figure11. Capacitance

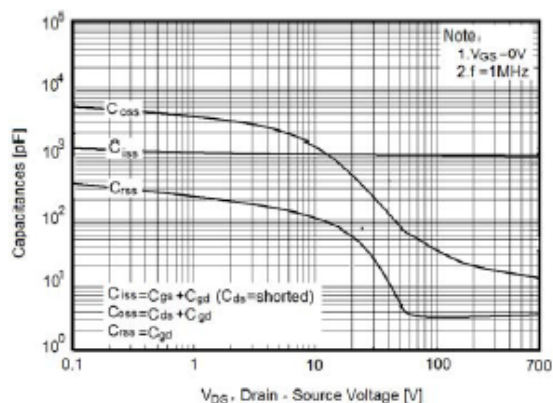
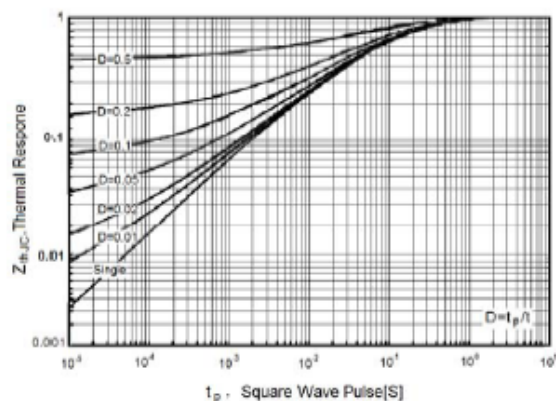


Figure12. Transient Thermal Impedance



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